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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	14

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

pnq

Office Action Summary	Application No. 09/265,119	Applicant(s) PERI ET AL.	
	Examiner Ayal I Sharon	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *13* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Introduction

1. Claims 1-20 of U.S. Application 09/265,119 were filed on 03/09/1999, with a Foreign Priority filing date of 9/30/98. A Request for Reconsideration, Declaration, and IDS (papers #11-13) were filed on 3/27/2003. An amendment (paper #9) was filed on 11/7/2002. Claim 9 was cancelled in the amendment, and Claim 8 was amended.

105 Response

2. In papers #7 and #10, Examiner requested from Applicants to provide the following prior art:
   - The **patents** referred to in the article provided by the examiner "Onwards and Upwards: New developments in 8-bit Micros". Challenge: News and Views from STMicroelectronics, March 1999, p.2. (Item 'V' in the PTO-892 'Notice of Refernces Cited' form provided with paper #7)
   - Specification sheets or data sheets for the versions of the ST9 Microcontroller produced in the years 1994-1997.
3. Applicants' responses in papers #11-13 have satisfied the Examiner's requests. Examiner thanks the Applicants for providing the documents in paper #13, as

requested by Examiner in paper #10. In addition, Examiner has entered the Applicants' Declaration (paper #12).

4. Examiner has withdrawn all the relevant objections.

Oath/Declaration

5. In paper #7, Examiner requested clarification as to relationship of Misters Devin, Leconte, Demange, Aulas, Guedj, Cappelletti, and Maurelli to the claimed invention. These inventors were co-inventors with Mr. Brigati (a co-inventor of the instant invention) on other issued patents that were not disclosed by the Applicants of the instant application.
6. Applicants responded (paper #9, p.13) that they "see no need to look behind the face of this duly executed declaration, and accordingly state that, on its face the duly executed declaration shows that 'Misters Devin, Leconte, Demange, Aulas, Guedj, Cappelletti, and Maurelli' bear no relationship to the claimed invention."
7. Examiner has withdrawn the objection.

Drawings

8. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Specification

9. In paper #9, pp.1-2, Applicants' amended the title of the instant application, as requested by the Examiner. Examiner's has consequently withdrawn the objection to the specification.

Claim Interpretations

10. In paper #7, Examiner interpreted a "Flash" memory structure as being a "flash EEPROM" as described in Brigati et al., U.S. Patent 6,011,717, Col. 1, lines 24-31. Examiner also interpreted "Flash EPROM" as being a set of devices that include "flash EEPROM".

11. In paper #9, p.14, the Applicants requested that "the pending claims ... be 'given the broadest reasonable interpretation consistent with the specification.'" As mandated by MPEP §2113.

12. Examiner is providing the following definitions in order to clarify the definitions of the terms.

- According to the Lee et al., U.S. Patent 5,777,923 (col. 1, lines 13-19):

> "In essence, a flash memory is an electrically erasable programmable read only memories (EEPROM) that supports three operations: read, program and erase."

- According to the Lee et al., U.S. Patent 5,777,923 (col. 1, lines 49-54):

> "Known flash memories have several drawbacks. Some known flash memories perform block program and erase functions to initialize the entire memory into a predetermined state prior to programming the memory with new data. There is no flexibility to select arbitrary words or bits within a block to be efficiently erased or programmed. An example is given in Table 1."

Therefore, Examiner interprets the difference between EEPROM and Flash to be that Flash can only be erased one block at a time, whereas EEPROM enables smaller element sizes to be erased.

Claim Objections

13. Examiner acknowledges Applicants' amendment (paper #9) to Claim 8 to incorporate the limitations of the then-pending Claim 9, as well as the cancellation of the then-pending Claim 9. Examiner's objection to Claim 9 has therefore been rendered moot, and has been withdrawn.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

15. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

16. The prior art used for these rejections is as follows:

- Lee et al., U.S. Patent 5,777,923. (Henceforth referred to as "**Lee**")

17. Claims 1-8 and 10-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee.

18. In regards to Claim 1, Lee teaches the following limitations:

> 1. An emulated EEPROM memory device, comprising a memory macrocell which is embedded into an integrated circuit having a microcontroller,
> (Lee, especially: col.2, lines 45-65; Fig.1 and associated text)
>
> the memory macrocell including a Flash memory structure formed by a predetermined number of sectors, wherein at least two sectors of the Flash memory structure are structured to emulate EEPROM byte alterability.
> (Lee, especially: col.2, lines 45-65; Fig.1 and associated text)

19. In regards to Claim 2, Lee teaches the following limitations:

> 2. The emulated EEPROM memory device according to claim 1, wherein said EEPROM byte alterability is emulated by hardware means,
> (Lee, especially: col.2, lines 45-65; Fig.1 and associated text)

20. In regards to Claim 3, Lee teaches the following limitations:

> 3. The emulated EEPROM memory device according to claim 1, wherein 8 Kbyte of the Flash memory structure are used to emulate 1 Kbyte of an EEPROM memory portion
> (Lee, especially: Fig. 2A, 2B and associated text)

21. In regards to Claim 4, Lee teaches the following limitations:

> 4. The emulated EEPROM memory device according to claim 1, wherein first and second EEPROM emulated sectors are each divided in a pre-determined number of blocks of the same size and each block is divided in pages.
> (Lee, especially: "block" – col.15, line 60 – col.16, line 7;
> "page" – Fig.7; col. 7, lines 42-62; col.10, lines 10-21)

22. In regards to Claim 5, Lee teaches the following limitations:

> 5. The emulated EEPROM memory device according to claim 1,
>
> wherein a state machine is provided for controlling an address counter which is output connected to an internal address bus running inside the memory macrocell,
> (Lee, especially: col.2, line 45 to col.3, line 7)

said address counter receiving control signals from the state machine in order to control the loading of hard-coded addresses in volatile or non-volatile registers which are read and updated by the microcontroller during a reset phase or by the state machine after an EEPROM update.
(Lee, especially: col.2, line 45 to col.3, line 7)

23. In regards to Claim 6, Lee teaches the following limitations:

6. The emulated EEPROM memory device according to claim 5,

wherein said internal address bus is connected to the input of a RAM buffer which is used for the page updating of the EEPROM including two additional byte for storing a page address during a page updating phase.
(Lee, especially: Fig.3; col.6, lines 13-20)

24. In regards to Claim 7, Lee teaches the following limitations:

7. The emulated EEPROM memory device according to claim 1, wherein Flash and EEPROM memories operations are controlled through a register interface mapped into the memory.
(Lee, especially: col.2, line 45 to col.3, line 7)

The "decoders" act the interface mapping to the memory.

25. In regards to Claim 8, Lee teaches the following limitations:

8. A method for emulating features of an EEPROM memory device incorporated into a memory macrocell which is embedded into an integrated circuit that also includes a microcontroller and a Flash memory structure formed by a predetermined number of sectors,
(Lee, especially: col.2, lines 45-65; Fig.1 and associated text)

comprising using at least two sectors of the Flash memory structure to emulate EEPROM byte alterability
(Lee, especially: col.2, lines 45-65; Fig.1 and associated text)

by dividing each of said at least two sectors into a pre-determined number of blocks of the same size and each block into a pre-determined number of pages
(Lee, especially: col.2, lines 45-65; Fig.1 and associated text;
Fig.7; col. 7, line 42 to col.7, line 62; col.15, line 60 to col.16, line 7)

and updating the emulated EEPROM memory portion programming different memory locations in a single bit mode.
(Lee, especially: col.2, lines 45-65; Fig.1 and associated text)

wherein at a page update selected page data are moved to a next free block and, when an EEPROM sector is full, all the pages are swapped to the another EEPROM sector.
(Lee, especially: Fig. 8B; col.7, line 62 – col.8, line 14)

26. In regards to Claim 9, it was cancelled by the Applicants in paper #9.

27. In regards to Claim 10, Lee teaches the following limitations:

> 10. A Flash memory device for emulating an EEPROM, comprising:
>
> first and second Flash memory portions each including plural memory blocks with plural memory locations, each of the memory locations sharing an address with a corresponding memory location in each of the blocks of the first and second Flash memory portions. all of the memory locations sharing a same address being a set of memory locations; and
> (Lee, especially: Figs.7-8; col.7, line 42 to col.8, line 14)
>
> a plurality of memory pointers each reflecting which memory block includes a current memory location for a set of memory locations, each set of memory locations including a current memory location; and
> (Lee, especially: Figs.7-8; col.7, line 42 to col.8, line 14)
>
> a memory controller structured to, in response to receiving a request to write data to a selected address assigned to a selected one of the sets of memory locations, determine from a memory pointer associated with the selected address which memory location in the selected set is a next memory location following the current memory location for the selected set and write the data in the next memory location.
> (Lee, especially: Figs.7-8; col.7, line 42 to col.8, line 14)

The use of page addresses and page pointers is inherent in a process involving storing and loading pages and sub-pages. Without addresses and pointers, it is impossible to keep track of the pages and sub-pages being repeated stored and loaded, as taught in the cited section of Lee.

28. In regards to Claim 11, Lee teaches the following limitations:

> 11. The Flash memory device of claim 10 wherein the first and second Flash memory portions are part of first and second memory sectors, the first memory sector including a first set of the plurality of memory pointers associated with the first Flash memory portion and the second memory sector including a second set of the plurality of memory pointers associated with the second Flash memory portion.
> (Lee, especially: Figs.7-8; col.7, line 42 to col.8, line 14)

The use of page addresses and page pointers is inherent in a process involving storing and loading pages and sub-pages. Without addresses and pointers, it is

impossible to keep track of the pages and sub-pages being repeated stored and loaded, as taught in the cited section of Lee.

29. In regards to Claim 12, Lee teaches the following limitations:

> 12. The Flash memory device of claim 10 wherein each block includes a plurality of memory pages with each memory page including a plurality of the memory locations and each of the memory pointers is a page pointer associated with a respective one of the memory pages.
> (Lee, especially: Figs.7-8; col.7, line 42 to col.8, line 14)

The use of page addresses and page pointers is inherent in a process involving storing and loading pages and sub-pages. Without addresses and pointers, it is impossible to keep track of the pages and sub-pages being repeated stored and loaded, as taught in the cited section of Lee.

30. In regards to Claim 13, Lee teaches the following limitations:

> 13. The Flash memory device of claim 12 wherein the plurality of Flash memory portions include two Flash memory portions, each with four memory blocks, each memory block including 64 memory pages each with 16 memory locations that are able to store a data byte.
> (Lee, especially: Figs.7-8; col.7, line 42 to col.8, line 14)

The use of page addresses and page pointers is inherent in a process involving storing and loading pages and sub-pages. Without addresses and pointers, it is impossible to keep track of the pages and sub-pages being repeated stored and loaded, as taught in the cited section of Lee.

31. In regards to Claim 14, Lee teaches the following limitations:

> 14. The Flash memory device of claim 10, further including a third Flash memory portion not organized to emulate the EEPROM.
> (Lee, especially: Figs.7-8; col.7, line 42 to col.8, line 14)

32. In regards to Claim 15, Lee teaches the following limitations:

> 15. The Flash memory device of claim 14, further including first and second sense amplifiers, the first sense amplifier being coupled to, and structured to read, the first and second Flash

memory portions and the second sense amplifier being coupled to, and structured to read, the third Flash memory portion.
(Lee, especially: Figs.7-8; col.7, line 42 to col.8, line 14)

A transistor is an amplifier. As clearly shown in the figures, the circuits in Lee are made with transistors.

33. In regards to Claim 16, Lee teaches the following limitations:

16. A method of emulating an EEPROM using Flash memory, the method comprising:

dividing the Flash memory into first and second memory sectors each including a plurality of memory blocks, each memory block including plural memory pages each with plural memory locations;
(Lee, especially: Fig.1, Items 12a-j; "Block Erase/Program Option" – col.15, line 60 to col.16, line 7; Fig.7 and associated text in col.7, lines 42-62)

assigning to each memory page of the first and second memory sectors a page address that is shared by a corresponding page in each of the memory blocks of the first and second memory sectors;
(Lee, especially: Fig.7 and associated text in col.7, lines 42-62)

in response to a first write instruction to write to a selected page address, writing to a data page of a first memory block of the first memory sector; and
(Lee, especially: Fig.7 and associated text in col.7, lines 42-62)

in response to a second write instruction to write data to the selected page address, writing to a data page of a second memory block of the first memory sector.
(Lee, especially: Fig.7 and associated text in col.7, lines 42-62)

34. In regards to Claim 17, Lee teaches the following limitations:

17. The method of claim 16, further comprising, in response to a third write instruction to write to the selected page address when a most recent write instruction to write to the selected page address was executed by writing to a last memory block of the first memory sector, executing the third write instruction by writing to a first memory block of the second memory sector.
(Lee, especially: Fig.7 and associated text in col.7, lines 42-62)

35. In regards to Claim 18, Lee teaches the following limitations:

18. The method of claim 16 wherein all memory pages sharing a same page address constitute a set of memory pages, the number of sets of memory pages equaling how many memory pages are in each memory block, the method further comprising:
(Lee, especially: Figs.7-8; col.7, line 42 to col.8, line 14)

assigning to each set of memory pages of the first and second memory sectors a page pointer that reflects which memory page in the set has been most recently updated; and
(Lee, especially: Figs.7-8; col.7, line 42 to col.8, line 14)

in response to each write instruction requesting to write data to the selected page address, determining which page pointer is associated with the selected page address, determining from the page pointer associated with the selected page address which memory page of the set of memory pages assigned the selected page address is next to be updated, and writing the data in the memory page that is determined to be the next memory page to be updated.
(Lee, especially: Figs.7-8; col.7, line 42 to col.8, line 14)

The use of page addresses and page pointers is inherent in a process involving storing and loading pages and sub-pages. Without addresses and pointers, it is impossible to keep track of the pages and sub-pages being repeated stored and loaded, as taught in the cited section of Lee.

36. In regards to Claim 19, Lee teaches the following limitations:

19. The method of claim 16, further comprising erasing the second memory sector while updating memory pages of the first memory sector.
(Lee, especially: Fig.7 and associated text in col.7, lines 42-62)

37. In regards to Claim 20, Lee teaches the following limitations:

20. The method of claim 19 wherein the erasing act is performed in plural erase phases, with each of the erase phases being triggered by writing data in the first memory sector.
(Lee, especially: Fig.7 and associated text in col.7, lines 42-62)

Response to Amendment

Applicants' Arguments Re: Claim Rejections - 35 USC § 112

38. Examiner (paper #7) issued a 35 USC 112 2nd paragraph rejection of Claims 1,8 and their respective dependent claims on the basis of lack of definiteness. Applicant has used the term "predetermined number" without specifying what that

number is (e.g. "predetermined number of sectors", "predetermined number of blocks", "predetermined number of pages").

39. Applicants' argument (paper #9, p.12) is that the term "predetermined number" in a claim, even when lacking an antecedent in the specification, makes the term broad and not indefinite.

As evidence for this argument, Applicants refer the Examiner to issued U.S. Patents 6,473,879 (to Ishii) and 6,473,878 (to Wei), which use the words "predetermined number" without reciting what the number is.

40. In response to Applicants' reference to two specific patents, Examiner refers the Applicants to MPEP §1701, which states that:

> "Public policy demands that every employee of the United States Patent and Trademark Office (USPTO) refuse to express to any person any opinion as to the validity or invalidity of, or the patentability or unpatentability of any claim in any U.S. patent, except to the extent necessary to carry out
> (A) an examination of a reissue application of the patent,
> (B) a reexamination proceeding to reexamine the patent, or
> (C) an interference involving the patent."

Thus the Examiner has not considered the two patents cited by the Applicants.

41. Examiner has re-evaluated the specification, and has found that lines from p.5, line 27 to p.6, line 3 provide sufficient support for the claims. Therefore the claims are broad, as the Applicant argues, as opposed to being indefinite. The rejections have been withdrawn.

Applicants' Arguments Re: Claim Rejections - 35 USC § 102

42. Applicants argue (paper #9) that U.S. Patent 5,991,199 ("Brigati") does not teach the claimed limitations of Claims 1, 8, 16 and their dependant claims. Examiner has located a reference ("Lee") that more clearly teaches the claimed limitations.

43. All rejections based on the Brigati reference have been withdrawn and replaced with rejections based on the Lee reference.

Applicants' Arguments Re: Claim Rejections - 35 USC § 103

44. Applicants argue (paper #9) that U.S. Patent 6,141,254 ("Devin") does not teach any of the claimed limitations of Claims 10-15. Examiner has located a reference ("Lee") that more clearly teaches the claimed limitations.

45. All rejections based on the Devin reference have been withdrawn and replaced with rejections based on the Lee reference.

Conclusion

46. This action is non-final.

47. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure. All of the following patents describe emulating EEPROM features on Flash memory.

48. Matsubara et al., U.S. Patent 5,687,345.

49. Matsubara et al., U.S. Patent 5,581,503.

50. Nishikata et al., U.S. Patent 5,699,546.

51. Tomoeda. U.S. Patent 5,574,684.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

The fax phone numbers for the organization where this application or proceeding is assigned are:

Official communications:	(703) 746-7239
Non-Official / Draft communications	(703) 746-7240
After Final communications	(703) 746-7238

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

June 12, 2003

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER